

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Sharad Saxena et al.

Serial No.: 09/675,427

Group Art Unit: 2128

Filed: September 29, 2000

Examiner: Morella Rosales Hanner

For: AN EFFICIENT METHOD FOR MODELING AND SIMULATION OF THE
IMPACT OF LOCAL AND GLOBAL VARIATION OF INTEGRATED CIRCUITS

I hereby certify that this correspondence is being deposited
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22313-1450

August 23, 2004
Date Steven E. Koffs
Steven E. Koffs, Registration No. 37,163

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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AUG 27 2004

Dear Sir:

Technology Center 2100

Enclosed herewith is an Supplemental Information Disclosure Statement
pursuant to 37 CFR. § 1.56 in connection with the above-identified application, which
statement is being filed:

- ☐ Together with the present application.
- ☐ Before the first Office Action on the merits or three (3) months from the
filing date of this application, whichever occurs last. **[37 CFR § 1.97(b)]**
- ☒ After the first Office Action on the merits, but before a Final Office Action
under §1.113 or Notice of Allowance under §1.311, whichever occurs first.
[37 CFR § 1.97(c)]
- ☐ After a Final Office Action under §1.113 or Notice of Allowance under
§1.311, but prior to or with payment of the Issue Fee. **[37 CFR § 1.97(d)]**

Consistent with Applicant's obligations pursuant to 37 CFR §§1.97 and 1.98, the following requirements have been met:

☐ No separate requirements are needed.

☐ No additional fee is required.

☒ **Fee Under 37 CFR § 1.97(c)**

The fee of \$180.00 for submission of an IDS under § 1.97(c) as set forth in § 1.17(p) accompanies this statement.

☐ **Fee Under 37 CFR § 1.97(d)**

The fee of \$180.00 for submission of an information disclosure statement under § 1.97(d) set forth in § 1.17(p) accompanies this statement.

☐ **Certification Under 37 CFR § 1.97(e)**

- ☐ Each item of information contained in this statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement; or
- ☐ No item of information contained in this statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in this statement was known to any individual designated in §1.56(c) more than three months prior to the filing of this statement.

Provision of Copies of References

☐ Copies of cited references which are U.S. Patents or U.S. Patent Application Publications are not required for this application, which has a filing date after June 30, 2003 (1276 OG 55, 5 August 2003).

☒ A copy of each of the references listed on the attached Form PTO-1449 is enclosed herewith and forms a part hereof.

☐ Partial Translations of References are enclosed herewith and form a part hereof.

- ☐ A copy of the European Search Report from a corresponding or related EPO application is enclosed herewith.
- ☐ A copy of the International Search Report from a corresponding or related PCT application is enclosed herewith.

Identification of Prior Application(s) In Which Listed Information Was Already Cited And For Which No Copies Are Submitted Or Need Be Submitted

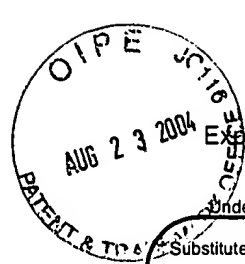
- ☐ This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior U.S. Application No(s). The following references were submitted to, and/or cited by, the Office in the prior application(s) and therefore are not required to be provided in this application:
- ☒ The Commissioner is hereby authorized to charge any fees associated with this communication or credit any overpayment to Deposit Account No. 04-1679. A duplicate copy of this transmittal is attached.

Respectfully submitted,

DATE: 8/23/04

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PTO/SB/08B (08-03)

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Application Number	09/675,427
Filing Date	September 29, 2000 AUG 27 2004
First Named Inventor	Sharad Saxena Technology Center 2100
Art Unit	2128
Examiner Name	Morella I Rosales Hanner
Attorney Docket Number	D5116-00002

Sheet

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of

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Y. CHENG et al., "MOSFET Modeling and BSIM User Guide." Kluwer Academic Publishers, Boston, 1999	<input checked="" type="checkbox"/>
		CONTI et al. "Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect." IEEE Transactions on Computer-Aided Design, Vol. 18, pp. 582-596, May 1999	<input type="checkbox"/>
		GUARDIANI et al., "Applying a submicron mismatch model to practical IC design." IEEE Custom Integrated Circuits Conference, San Diego (CA), May 1994	<input type="checkbox"/>
		HUIJISING et al., "Low-Power Low-Voltage VLSI Operational Amplifier Cells." IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 42, No. 11, pp. 841-852, November 1995	<input type="checkbox"/>
		HWANG, et al., "Universal Constant-gm Input-Stage Architectures for Low-Voltage Op Amps." IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 42, No. 11, pp. 886-894, November 1995.	<input type="checkbox"/>
		PINEDA DE GYVEZ et al., "Integrated Circuits Manufacturability: the Art of Process and Design Integration." pp. 158-166, IEEE Press, New York, 1999	<input type="checkbox"/>
		FELT et al., "Hierarchical Statistical Characterization of Mixed-Signal Circuits Using Behavioral Modeling." IEEE-ACM International Conference on Computer Aided Design, San Jose (CA), November 1996	<input type="checkbox"/>
		MICHAEL et al., "Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits." Kluwer Academic Publishers, Boston, 1993	<input type="checkbox"/>
		MICHAEL et al., "Statistical Modeling of Device Mismatch for Analog Integrated Circuits." IEEE Journal of Solid-State Circuits, Vol. 27, No. 2, February 1992	<input type="checkbox"/>
		"pdPCA User's Manual." Version ?, PDF Solutions, Inc., San Jose, 1998	<input type="checkbox"/>

Examiner
Signature

Date
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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